Module 4.
Data Converters
DAC and ADC

DATA CONVERTER INTEGRATED CIRCUITS

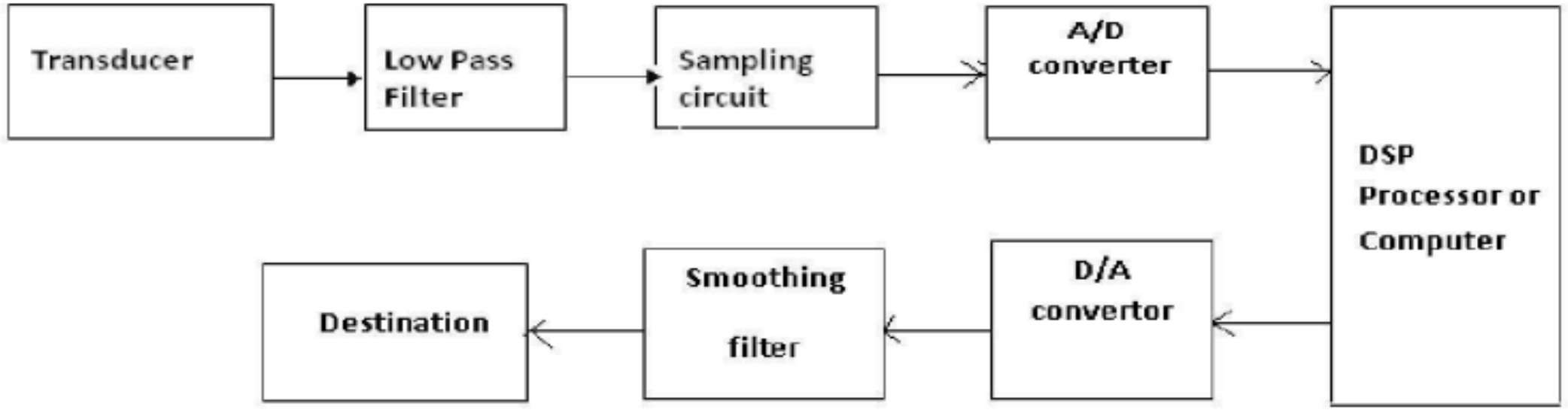


Fig: Application of A/D and D/A converters

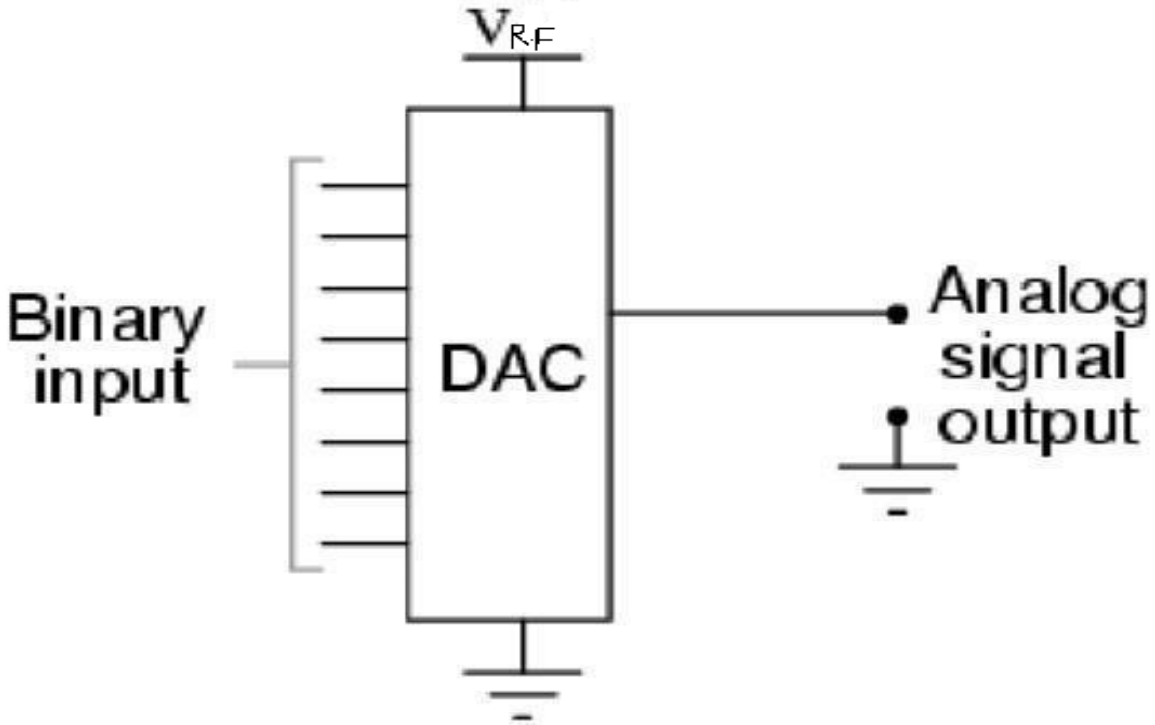
- The transducer circuit will gives an analog signal.
- This signal is transmitted through the LPF circuit to avoid higher components, and then the signal is sampled at twice the frequency of the signal to avoid the overlapping.

- The output of the sampling circuit is applied to A/D converter where the samples are converted into binary data i.e. 0's and 1's. Like this the analog data converted into digital data.

  The digital data is again reconverted back into analog by doing exact opposite operation of first half of the diagram. Then the output of the D/A convertor is transmitted through the smoothing filter to avoid the ripples.

BASIC DAC TECHNIQUES:

Fig: Basic DAC diagram



BASIC DAC TECHNIQUES

The input in the block diagram is binary data i.e, 0 and 1, it contain 'n' number of input bits designated as **d1,d2,d3,…..dn , this input is combined with the reference voltage** called Vref to give an analog output voltage.

Where, d1 is the MSB bit and dn is the LSB bit.

Vo = K.V_{FS} (d1*2^{-1}+ d2*2^{-2}+ d3*2^{-3}+……+ dn*2^{-n})

where, Vo = output voltage,

V_{FS} = Full scale deflection voltage, ie. when d1 d2 d3 =1 1 1

K= scaling factor set to 1.

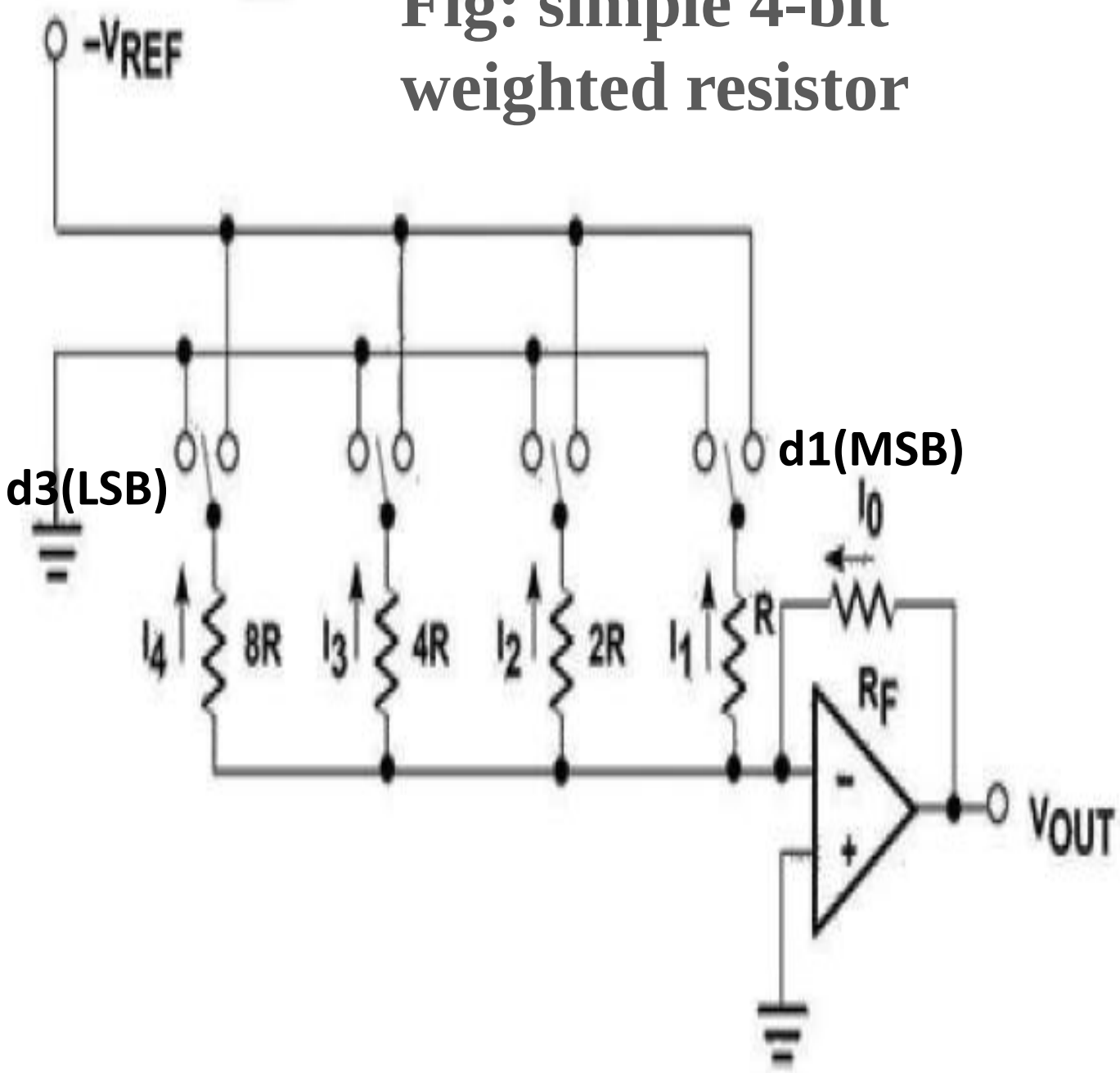


Fig: simple 4-bit weighted resistor

- Fig. shows a simplest circuit of weighted resistor. It uses a summing inverting amplifier. It contains n- electronic switches (i.e. 4 switches) and these switches are controlled by binary input bits d1, d2, d3, d4. If the binary input bit is 1 then the switch is connected to reference voltage –VREF , if the binary input bit is 0 then the switch is connected to ground. The output current equation is :

  Io = I1+ I2+ I3+ I4

  The output voltage

- Vo= Io * Rf

  $Vo = V_{REF} * (Rf/R)\,(d1*2^{-1} + d2*2^{-2} + d3*2^{-3} \text{----------} + dn*2^{-n})$

  Assume Rf/R= K =constant=1 and $V_{FS} = V_{REF}$

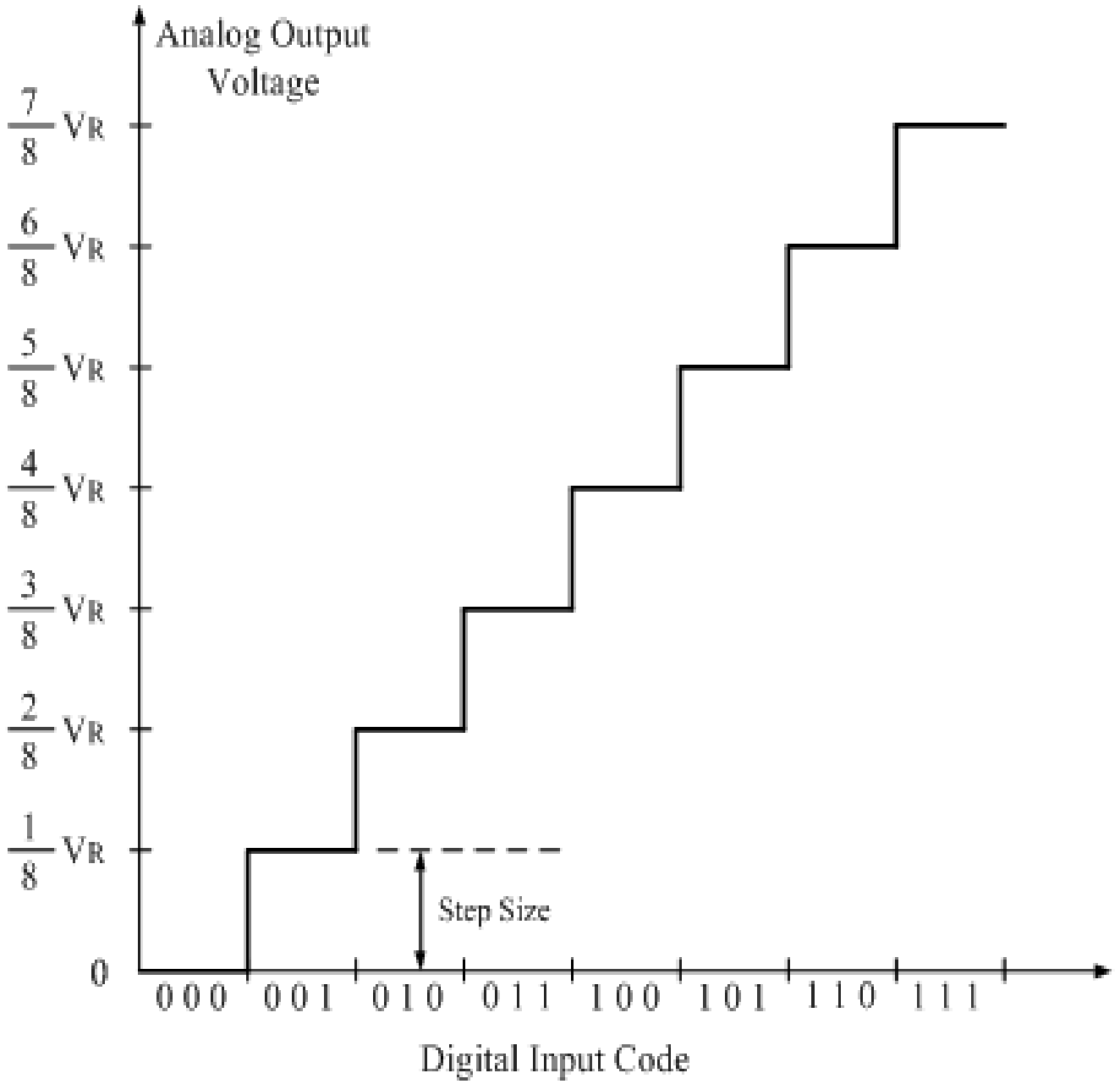
  $\mathbf{Vo = K.V_{FS}\,(d1*2^{-1} + d2*2^{-2} + d3*2^{-3} \ldots\ldots\ldots\ldots\ldots\ldots + dn*2^{-n})}$

  where, VFS = Full scale deflection voltage, For eg. when d1 d2 d3 =1 1 1

- The transfer characteristics and Truth Table are shown below (for a 3-bit weighted resistor).

Digital Input			Analog output voltage Vo	fOR VR =8V
d1	d2	d3		
0	0	0	0	0 V
0	0	1	VR/8	1 V
0	1	0	2 VR /8	2 V
0	1	1	3 VR /8	3 V
1	0	0	4 VR /8	4 V
1	0	1	5 VR /8	5 V
1	1	0	6 VR /8	6 V
1	1	1	7 VR /8	7 V

Fig: Transfer characteristics of 3-bit weighted resistor



Disadvantages of Weighted resistor D/A converter:

1) Wide range of resistor's are required in this circuit and it is very difficult to fabricate such a wide range of resistance values in monolithic IC.

ie. The difference between the resistance values corresponding to LSB & MSB will increase as the number of bits present in the digital input increases.

2) It is difficult to design more accurate resistors as the number of bits present in the digital input increases.

3) This difficulty can be eliminated using R-2R ladder network.

Specifications of DAC:

1) Resolution : It is defined as the smallest change in analog output voltage, when digital input advances by 1 state.

For eg. Digital input 1001 produce 9 V & 1010 produce 10 V then resolution = 1 V ie. Output increases in step of 1.

Its value depends on the number of bits in the digital input applied to DAC.

Higher the no of bits, higher (Better) the resolution.

Resolution should as high as possible.

Resolution can be defined in two different ways: Def) Resolution is the no. of different analog output voltage that can be provided by DAC. For n bit DAC is given by

Resolution = 2^n ---------- **equation 1**

Def 2) It is the ratio of change in analog output voltage, when digital input advances by 1 state.

Resolution = $\frac{V_{FS}}{2^n - 1}$ -------equation2 ------imp relation

Prob. Q1) 4- bit DAC has an output voltage range 0-5 V. calculate its resolution using both definitions of resolution. As per eqn 1 , the resolution is given by Resolution = 2^n = 2^4 = 16 = No of analog output voltages provided by DAC

As per def 2 :

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1} = \frac{5\ V}{2^4 - 1} = 0.333\ \text{V}$$

Thus the input change of 1 state causes the output change by 0.333 V.

MCQ: Q2) What is the resolution of a digital-to-analog converter (DAC) ?

Options are: A) It is the comparison between the actual output of the converter and its expected output.

B) It is the deviation between the ideal straight-line output and the actual output of the converter. C) It is the smallest analog output change that can occur because of an increment in the digital input.

D) It is its ability to resolve between forward and reverse steps when sequenced over its entire range.

Q4) A 6-bit ladder D/A converter has input 101001. For 0 = 0 V and 1 = 10V, the output is…. Options are: A) 4.23 V B) 5.52 V C) 6.51 V D) 9.23 V for Ans P.T.O.

Ans :-

$$Vo = VR\,(d1*2^{-1} + d2*2^{-2} + d3*2^{-3} + d4*2^{-4} + d5*2^{-5} + d62^{-6})$$

d1= d3 =d6 =1, d2=d4=d5=0

$$= 10\,(1*2^{-1} + 0*2^{-2} + 1*2^{-3} + 0*2^{-4} + 0*2^{-5} + 1*2^{-6})$$

= 10 (0.5 + 0 + 0.125 + 0 + 0 + 0.00156)

= 6.42

= 6.51 V , so option C is correct.

Que 2) Why the switches used in weighted resistor DAC are of single pole double throw (SPDT) type?

A) To connect the resistance to reference voltage

B) To connect the resistance to ground

C) To connect the resistance to either reference voltage or ground

D) To connect the resistance to output

Q3) A 10-bit D/A converter have an output range from 0-9v. Calculate the output voltage produced when the input binary number is 1110001010.

Options are: A) ± 7.96 V B) - 7.96 V C) 7.96 V D) 7.96 mV.

Ans= 7.96 V

2) Linearity: the relation between input and output should be linear. However Practically , it is not so due to error in the values of resistors used for the n/w

3) Accuracy:- the accuracy of DAC is a measure of how close the actual output voltage with the theoretical output voltage.

For eg. The digital input 1010 has to produce analog voltage of 10 V Theor.

But when we measure we get 9.8 V **4)Settling time:**

- **R-2R LADDER DAC:** Wide range of resistors required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC.
- The circuit of R-2R ladder network is shown in fig. The basic theory of the R-2R ladder network is that current flowing through any input resistor (2R) encounters two possible paths at the far end. The effective resistances of both paths are the same (also 2R), so the incoming current splits equally along both paths.
- The half-current that flows back towards lower orders of magnitude does not reach the op amp, and therefore has no effect on the output voltage.
- The half that takes the path towards the op amp along the ladder can affect the output. The inverting input of the op-amp is at virtual earth.
- Current flowing in the elements of the ladder network is therefore unaffected by switch positions. $V_o = K.\ V_{FS}/R\ (d1*2^{-1} + d2*2^{-2} + d3*2^{-3}$----------$+dn*2^{-n})$

  K =constant=1 and VFS = V_{REF} , VFS = Full scale deflection voltage,

- If we label the bits (or inputs) , bit 1 to bit N , the output voltage caused by connecting a particular bit to Vr with all other bits grounded is:

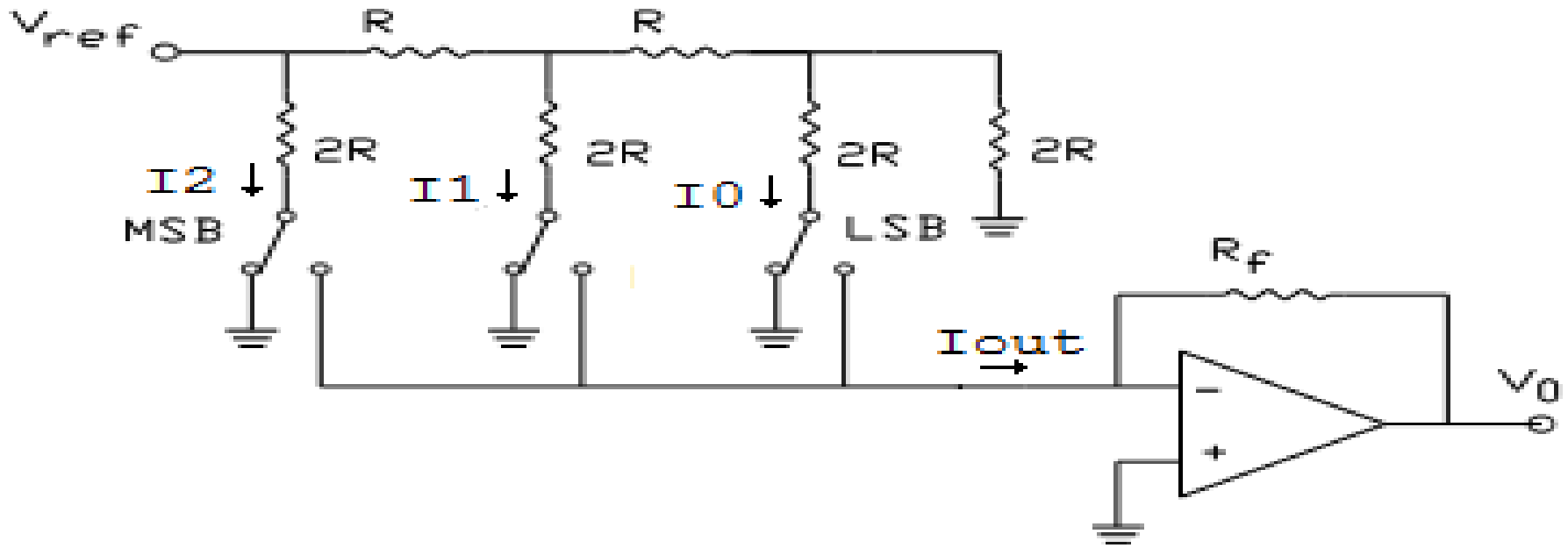
$$Vout = Vr /2N$$

where N is the bit number. For bit 1, Vout = Vr/2, for bit 2, Vout = Vr/4 etc.

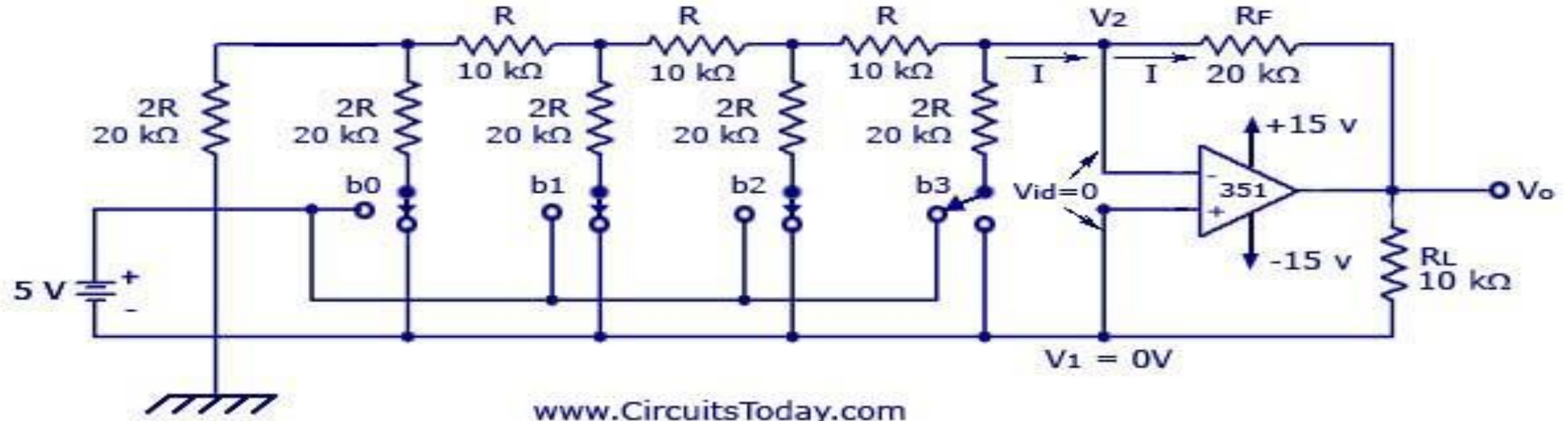
- Since an R/2R ladder is a linear circuit, we can apply the principle of superposition to calculate Vout. The expected output voltage is calculated by summing the effect of all bits connected to Vr. For example, if bits 1 and 3 are connected to Vr with all other inputs grounded, the output voltage is calculated by:

Vout = (Vr/2)+(Vr/8) which reduces to Vout = 5Vr/8.

- An R/2R ladder of 4 bits would have a full-scale output voltage of 1/2 +1/4 + 1/8 + 1/16 = 15Vr/16 or 0.9375 volts (if Vr=1 volt) while a 10bit R/2R ladder would have a full-scale output voltage of 0.99902 (if Vr=1 volt).

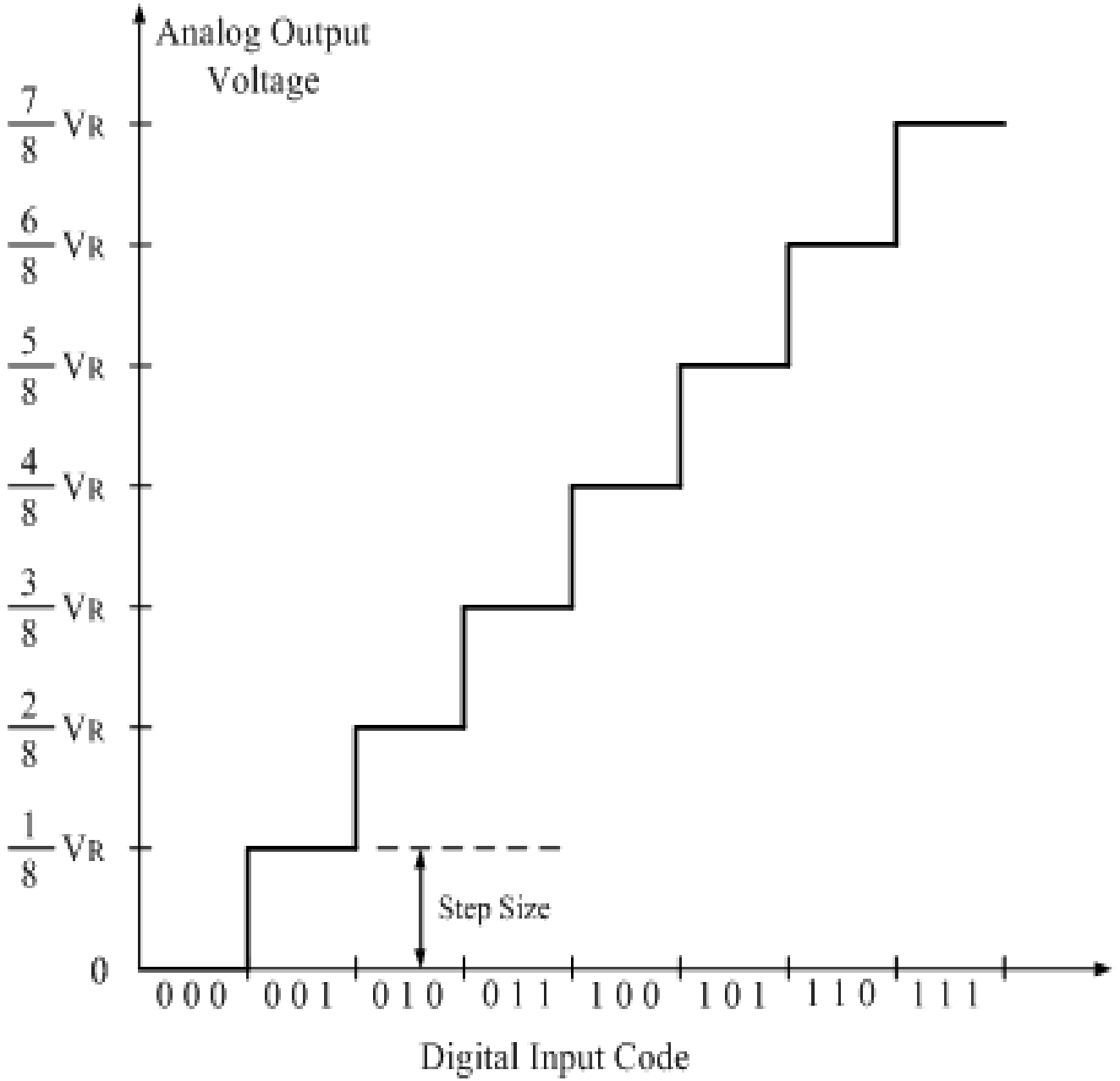


D/A Converter With R and 2R Resistors



Digital Input			Analog output voltage Vo	fOR V_R =8V
d1	d2	d3		
0	0	0	0	0 V
0	0	1	$V_R/8$	1 V
0	1	0	2 V_R /8	2 V
0	1	1	3 V_R /8	3 V
1	0	0	4 V_R /8	4 V
1	0	1	5 V_R /8	5 V
1	1	0	6 V_R /8	6 V
1	1	1	7 V_R /8	7 V

Fig: Transfer characteristics of 3-bit weighted resistor



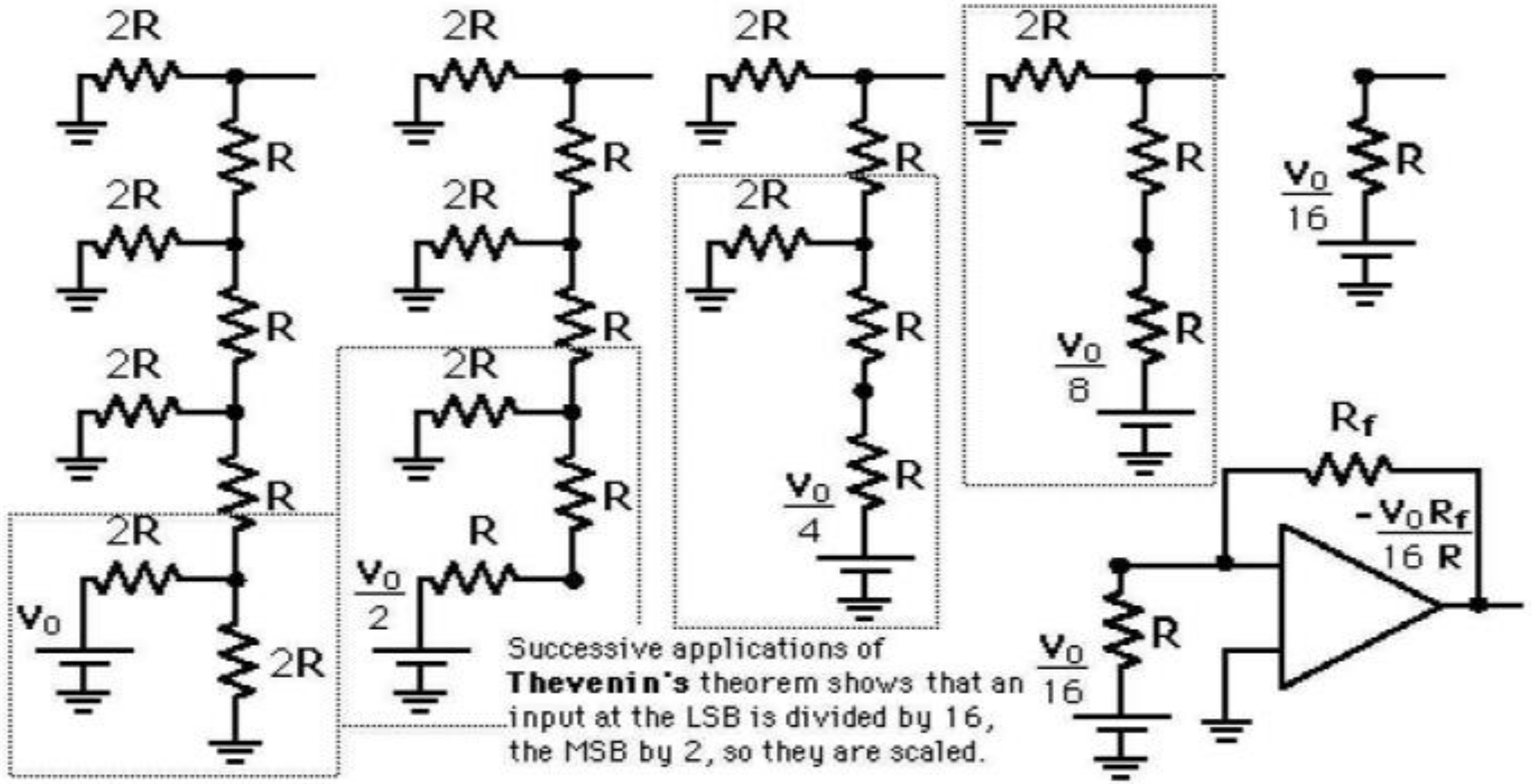


Fig: A 4-bit R-2R Ladder DAC

Q1) Only two values of resistors are required for which of the following types of DACs

Options are: A) Binary weighed DAC

B) Weighed resistor type of DAC

C) R-2R Ladder type DAC

D) All of the above

Q 2) Which of the following is a drawback of R-2R ladder type DAC

A) Lesser Word Length only can be used

B) Higher Values of resistances are required

C) Non-Linearity effects come in due to power dissipation

D) None of the above are drawbacks

INVERTED R-2R LADDER DAC

- In weighted resistor and R-2R ladder DAC the current flowing through the resistor is always changed because of the changing input binary bits 0 and 1. More power dissipation causes heating, which in turn cerates non-linearity in DAC. This problem can be avoided by using INVERTED R-2R LADDER DAC (fig 2.20)

- In this MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of op-amp which is also at virtual ground.
- When the input binary in logic 1 then it is connected to the virtual ground, when input binary is logic 0 then it is connected to the ground i.e. the current flowing through the resistor is constant.

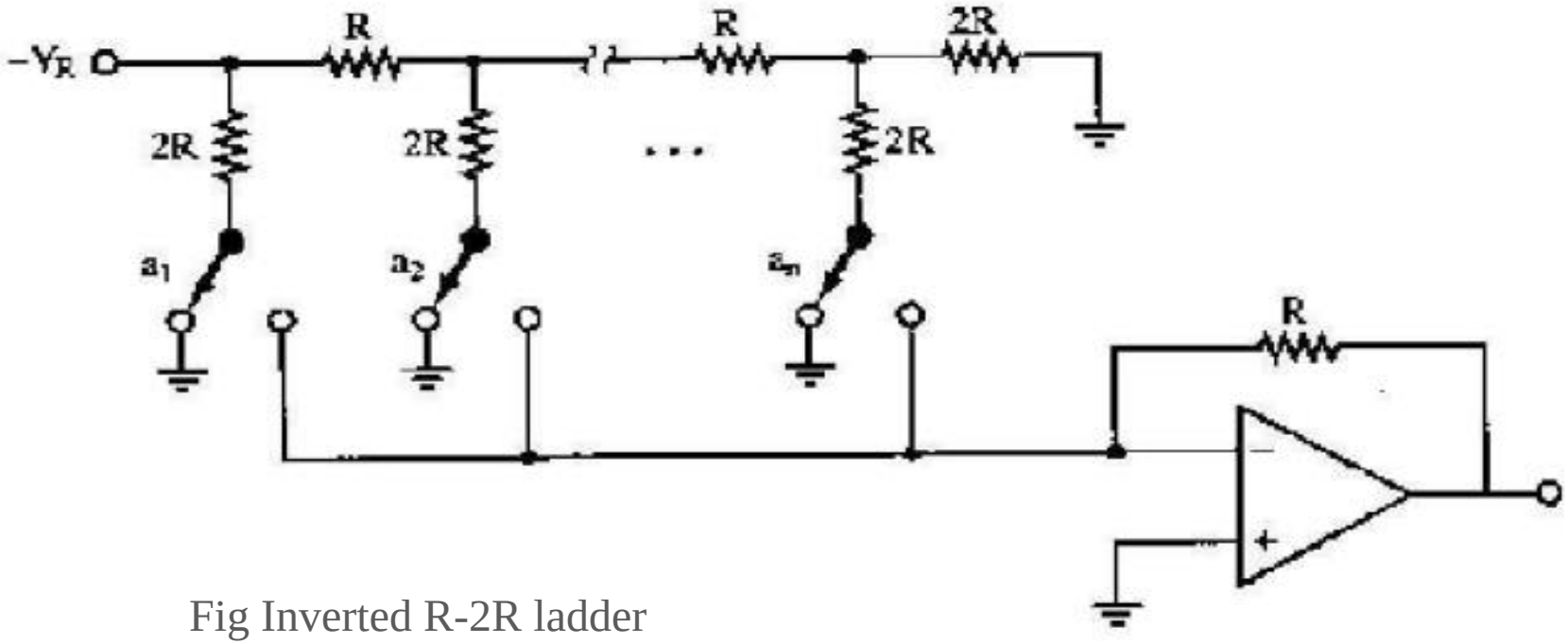


Fig Inverted R-2R ladder

CLASSIFICATION OF ADCS

1. Direct type ADC.
2. Integrating type ADC

Direct type ADCs

1. Flash (comparator) type converter
2. Counter type converter
3. Tracking or servo converter.
4. Successive approximation type converter.

INTEGRATING TYPE CONVERTERS

- An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time or frequency and then to a digital code is known as integrating type A/D converter

SAMPLE AND HOLD CIRCUIT

- A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems.

SAMPLE AND HOLD CIRCUIT

- The time during which the voltage across the capacitor in sample and hold circuit is equal to the input voltage is called sample period. The time period during which the voltage across the capacitor is held constant is called hold period

DIFFERENT TYPES OF ADC'S

- It provides the function just opposite to that of a DAC. It accepts an analog input voltage Va and produces an output binary word d1, d2,**d3….dn. Where d1 is the most significant bit and** dn is the least significant bit.
- ADCs are broadly classified into two groups according to their conversion techniques

  1)Direct type

  2)Integrating type

- Direct type ADCs compares a given analog signal with the internally generated equivalent signal.
  This group includes

1) Flash (Comparator) type converter
2) Successive approximation type convertor
3) Counter type

4)Servo or Tracking type

Integrated type ADCs perform conversion in an indirect manner by first changing the analog input signal to linear function of time or frequency and then to a digital code.

FLASH (COMPARATOR) TYPE CONVERTER

- A direct-conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, capable of gigahertz sampling rates, but usually has only 8 bits of resolution or fewer, since the number of comparators needed, 2N - 1, doubles with each additional bit, requiring a large, expensive circuit.
- ADCs of this type have a large die size, a high input capacitance, high power dissipation, and are prone to produce glitches at the output (by outputting an out-of-sequence code). Scaling to newer sub-micrometre technologies does not help as the device mismatch is the dominant design limitation. They are often used for video, wideband communications or other fast signals in optical storage.
- A Flash ADC (also known as a direct conversion ADC) is a type of analog-to-digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. Often these reference ladders are constructed of many resistors; however modern implementations show that capacitive voltage division is also possible.
- The output of these comparators is generally fed into a digital encoder which converts the inputs into a binary value (the collected outputs from the comparators can be thought of as a unary value).

- Also called the *parallel* A/D converter, this circuit is the simplest to understand. It is formed of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output.

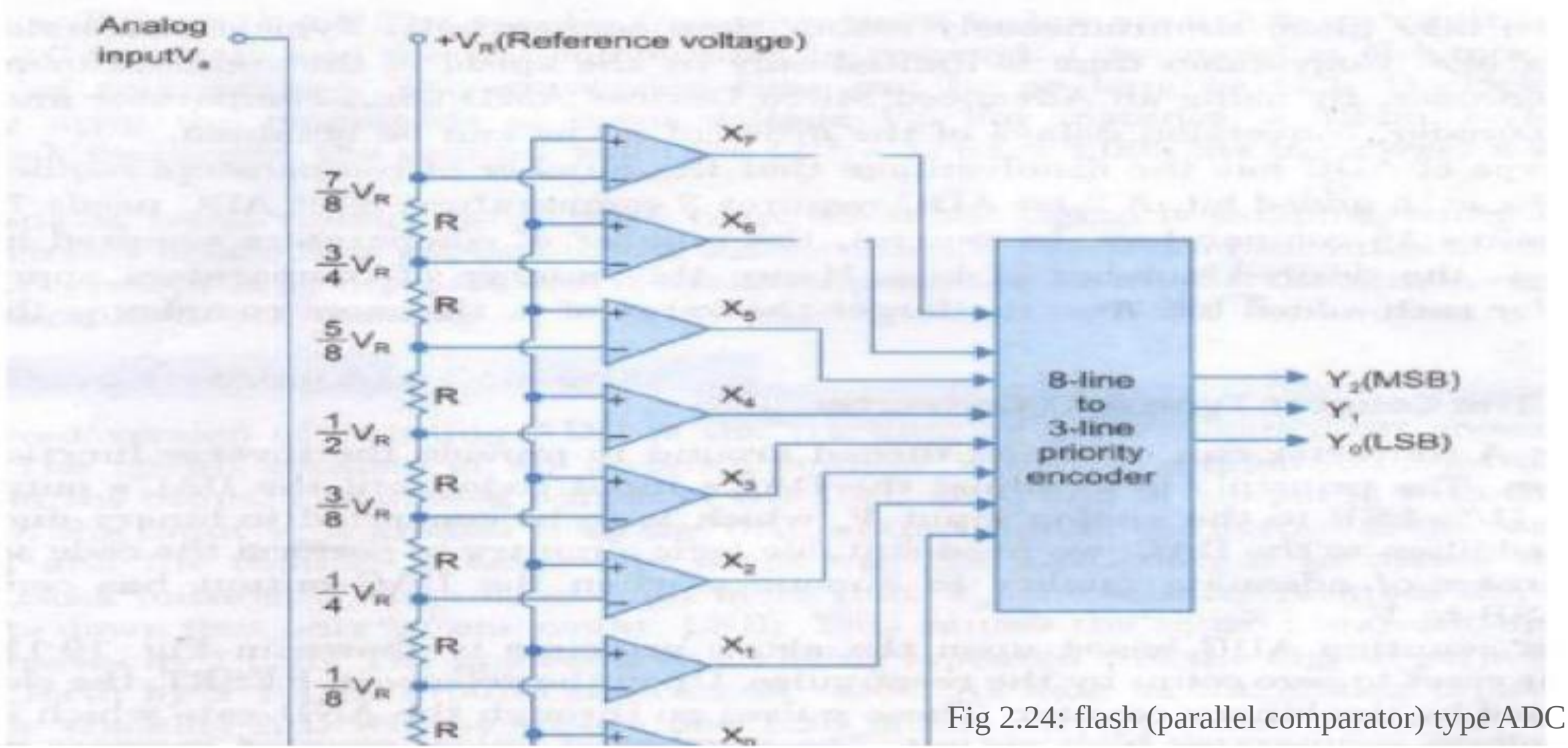
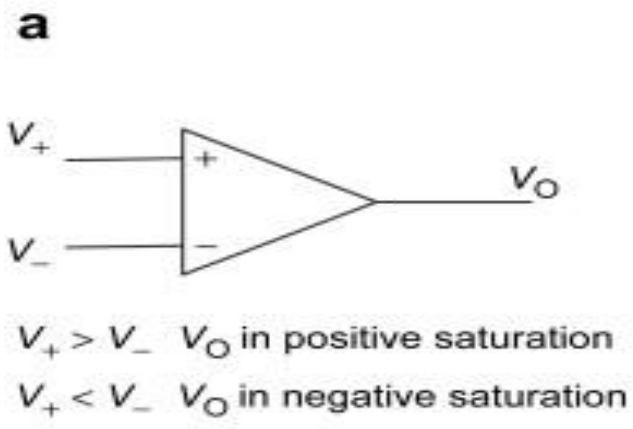
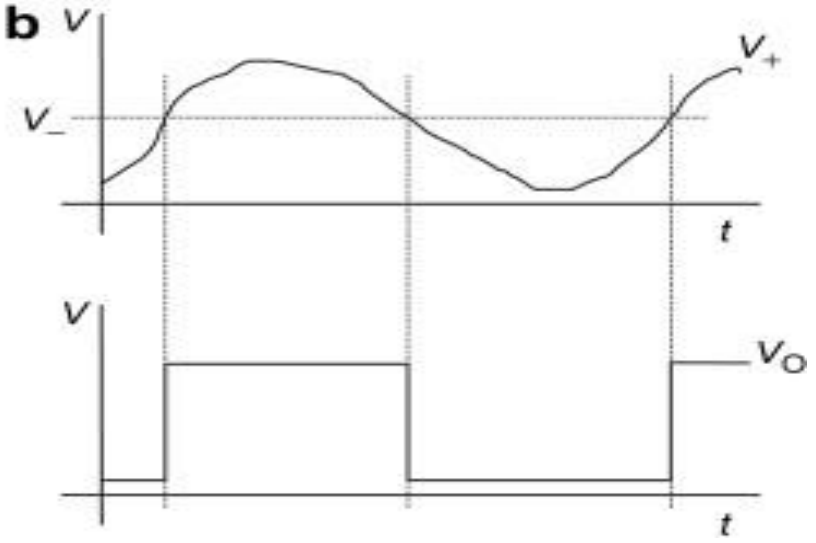


Fig 2.24: flash (parallel comparator) type ADC

Comparator Working:-

Voltage Input	Logic output
$V_1 > V_2$	X=1
$V_1 < V_2$	X=0
$V_1 = V_2$	Previous state





Input voltage	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
$0 - V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8 - V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4 - 3V_R/8$	0	0	0	0	0	1	1	1	0	1	0
$3V_R/8 - V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2 - 5V_R/8$	0	0	0	1	1	1	1	1	1	0	0
$5V_R/8 - 3V_R/4$	0	0	1	1	1	1	1	1	1	0	1
$3V_R/4 - 7V_R/8$	0	1	1	1	1	1	1	1	1	1	0
$7V_R/8 - V_R$	1	1	1	1	1	1	1	1	1	1	1

- VR is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit, not shown in the schematic.
- As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state.
- The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs.
- **MCQ : Q1) No of comparators required to build a 8-Bit flash type ADC is -----**

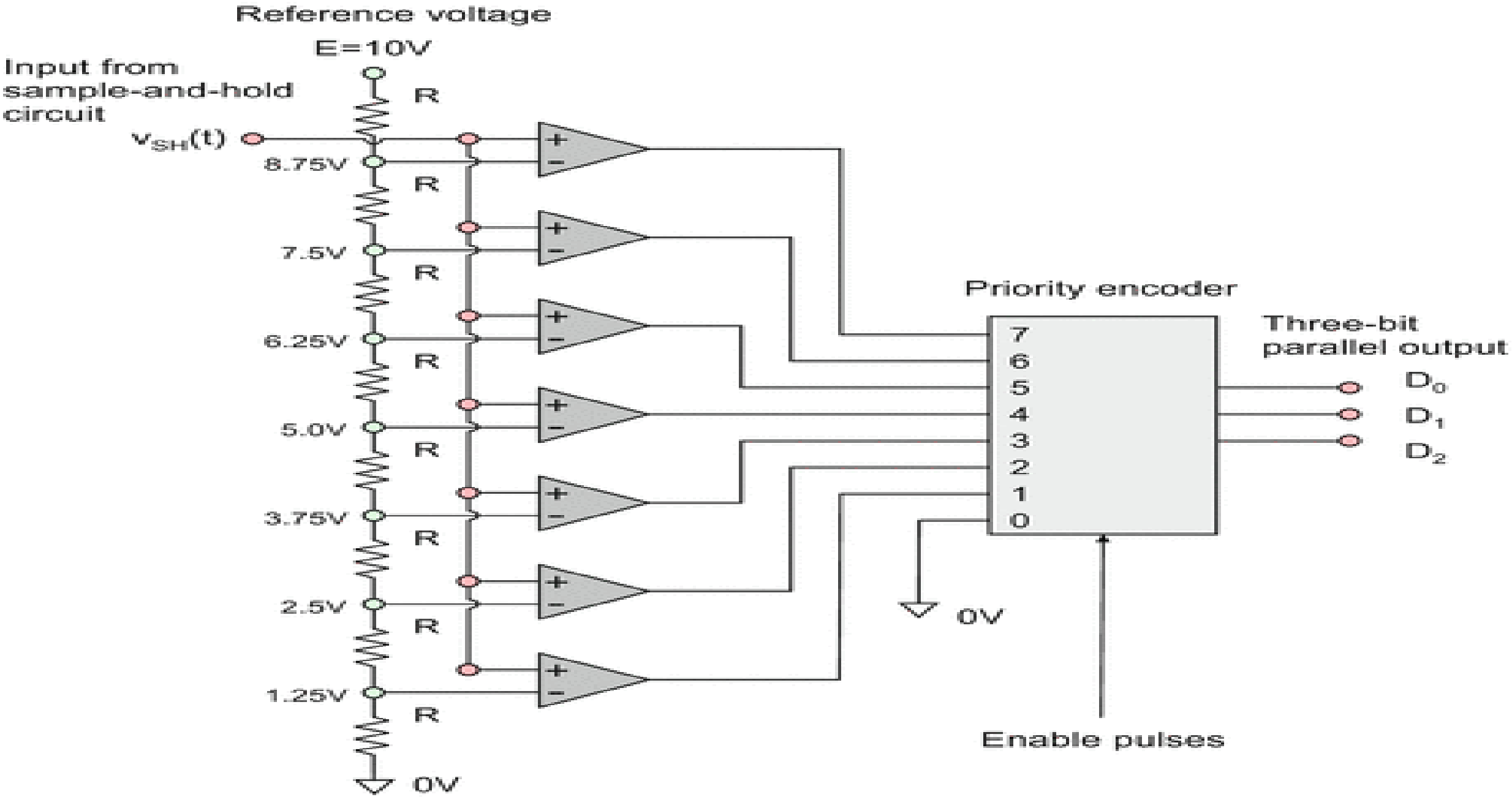
Options are : A) 256 B) 8 C) 255 D) 64

Q2) Find the resolution of a 10 bit ADC for an input range of 12 V.

A) 1.73 mV B) 111.73 mV C) 11.73 mV D) 1173 mV

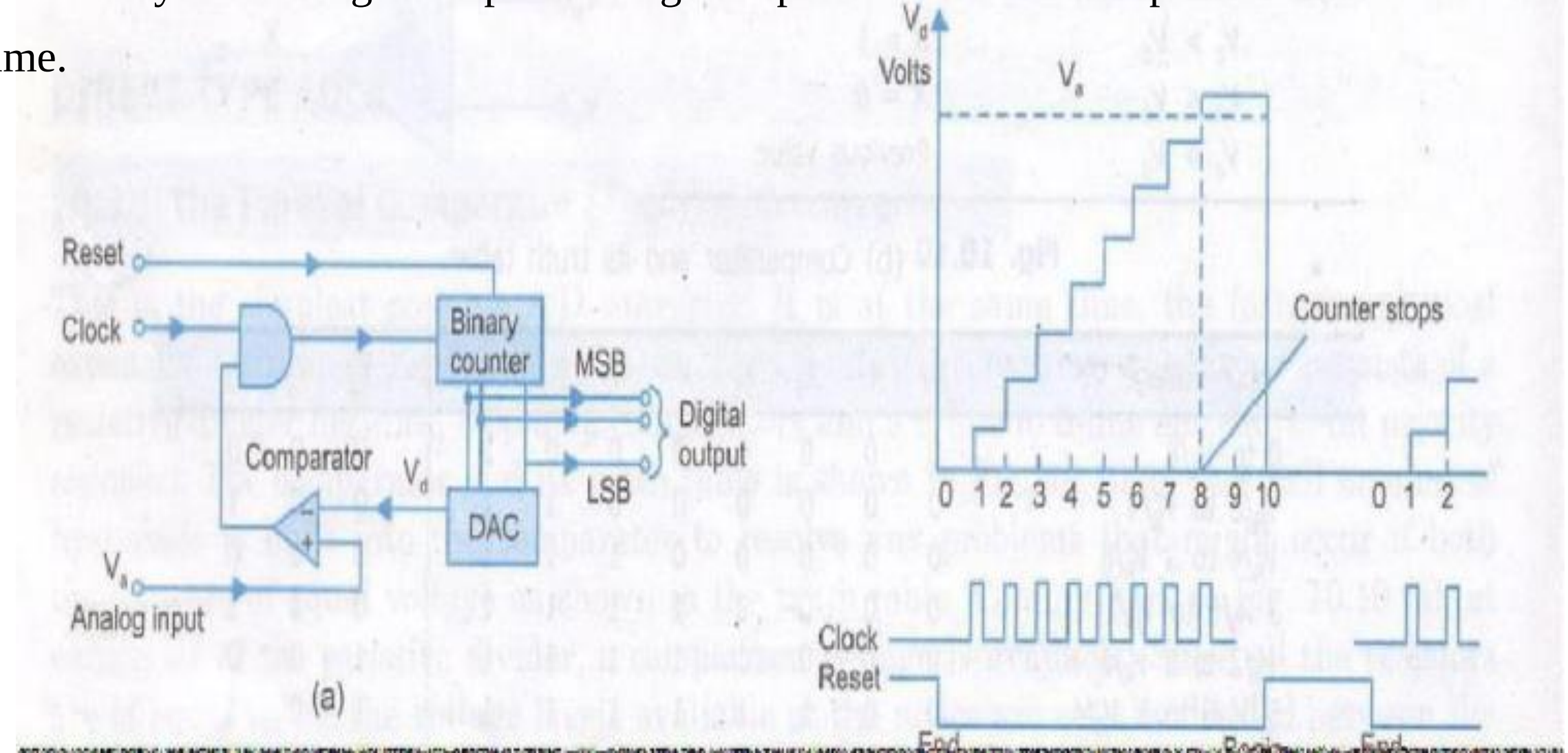
The only way to increase resolution without reducing the range is to use an ADC with more bits. A 10-bit ADC has 2^{10}, or 1,024 possible output codes. So the resolution is 5V/1,024, or 4.88mV; a 12-bit ADC has a 1.22mV resolution for this same reference.

Diagram of 3- bit Flash type ADC :-



COUNTER TYPE A/D CONVERTER

- In the fig. the counter is reset to zero count by reset pulse. After releasing the reset pulse the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time.

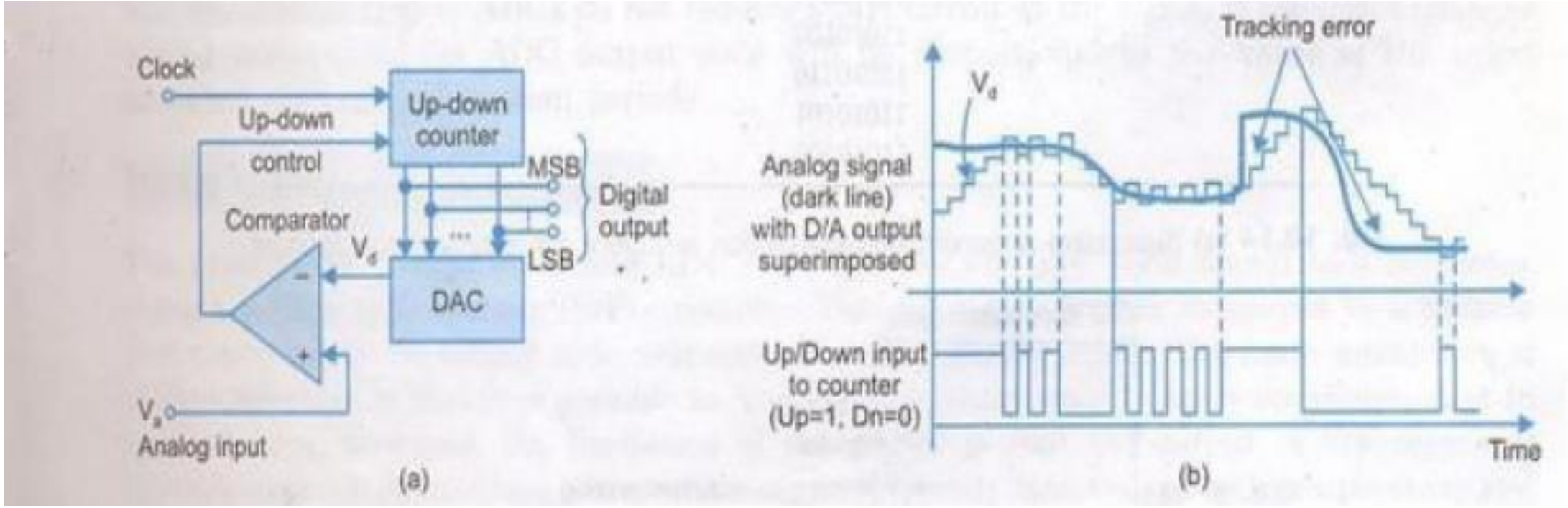


- **MCQ:** Q1) Find out the integrating type analog to digital converter from following options?
- Flash type converter
- Tracking converter
- Counter type converter
- Dual slope ADC

- The binary word representing this count is used as the input of a D/A converter whose output is a stair case. The analog output Vd of DAC is compared to the analog input input Va by the comparator. If Va>Vd the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter. When Va<Vd the output of the comparator becomes low and the AND gate is disabled. This stops the counting we can get the digital data.

SERVO TRACKING A/D CONVERTER

• An improved version of counting ADC is the tracking or servo converter shown in fig 2.23. The circuit consists of an up/down counter with the comparator controlling the direction of the count.



• The analog output of the DAC is Vd and is compared with the analog input Va. If the input Va is greater than the DAC output signal, the output of the comparator goes high and the counter is caused to count up. The DAC output increases with each incoming clock pulse when it becomes more than Va the counter reverses the direction and counts down.

SUCCESSIVE-APPROXIMATION ADC

- One method of addressing the digital ramp ADC's shortcomings is the so-called successive- approximation ADC. The only change in this design as shown in the fig 2.19 is a very special counter circuit known as a successive-approximation register.
- Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the most-significant bit and finishing at the least-significant bit.
- Throughout the count process, the register monitors the comparator's output to see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly.
- The way the register counts is identical to the "trial-and-fit" method of decimal-to-binary conversion, whereby different values of bits are tried from MSB to LSB to get a binary number that equals the original decimal number. The advantage to this counting strategy is much faster results: the DAC output converges on the analog signal input in much larger steps than with the 0-to-full count sequence of a regular counter.

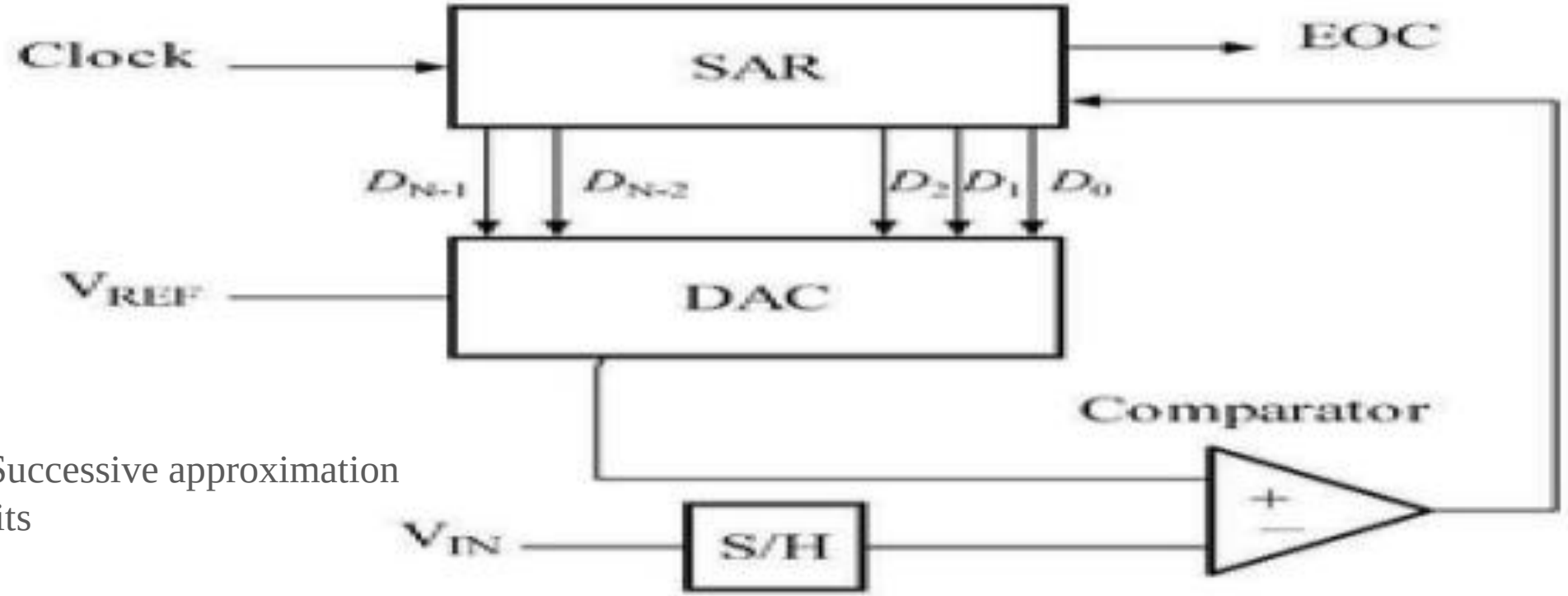


Fig: 2.27: Successive approximation ADC circuits

- The successive approximation analog to digital converter circuit typically consists of four chief sub

1. A sample and hold circuit to acquire the input voltage (Vin).

2. An analog voltage comparator that compares Vin to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR).

3. A successive approximation register sub circuit designed to supply an approximate digital code of Vin to the internal DAC.

4.An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with Vin.

- The successive approximation analog to digital converter circuit typically consists of four chief sub

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3. A successive approximation register sub circuit designed to supply an approximate digital code of Vin to the internal DAC.
4. 4.An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with Vin.

- The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code (Vref/2) into the comparator circuit for comparison with the sampled input voltage.
- If this analog voltage exceeds Vin the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested.
- The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC).

- Mathematically, let Vin = xVref, so x in [-1, 1] is the normalized input voltage. The objective is to approximately digitize x to an accuracy of 1/2n. The algorithm proceeds as follows:

1.Initial approximation x0 = 0.

2.ith approximation xi = xi-1 - s(xi-1 - x)/2i.

where, s(x) is the signum-**function(sgn(x)) (+1 for x ≥ 0,** -1 for x < 0). It follows using mathematical induction that |xn - **x| ≤ 1/2n.**

As shown in the above algorithm, a SAR ADC requires:

1.An input voltage source Vin.

2.A reference voltage source Vref to normalize the input.

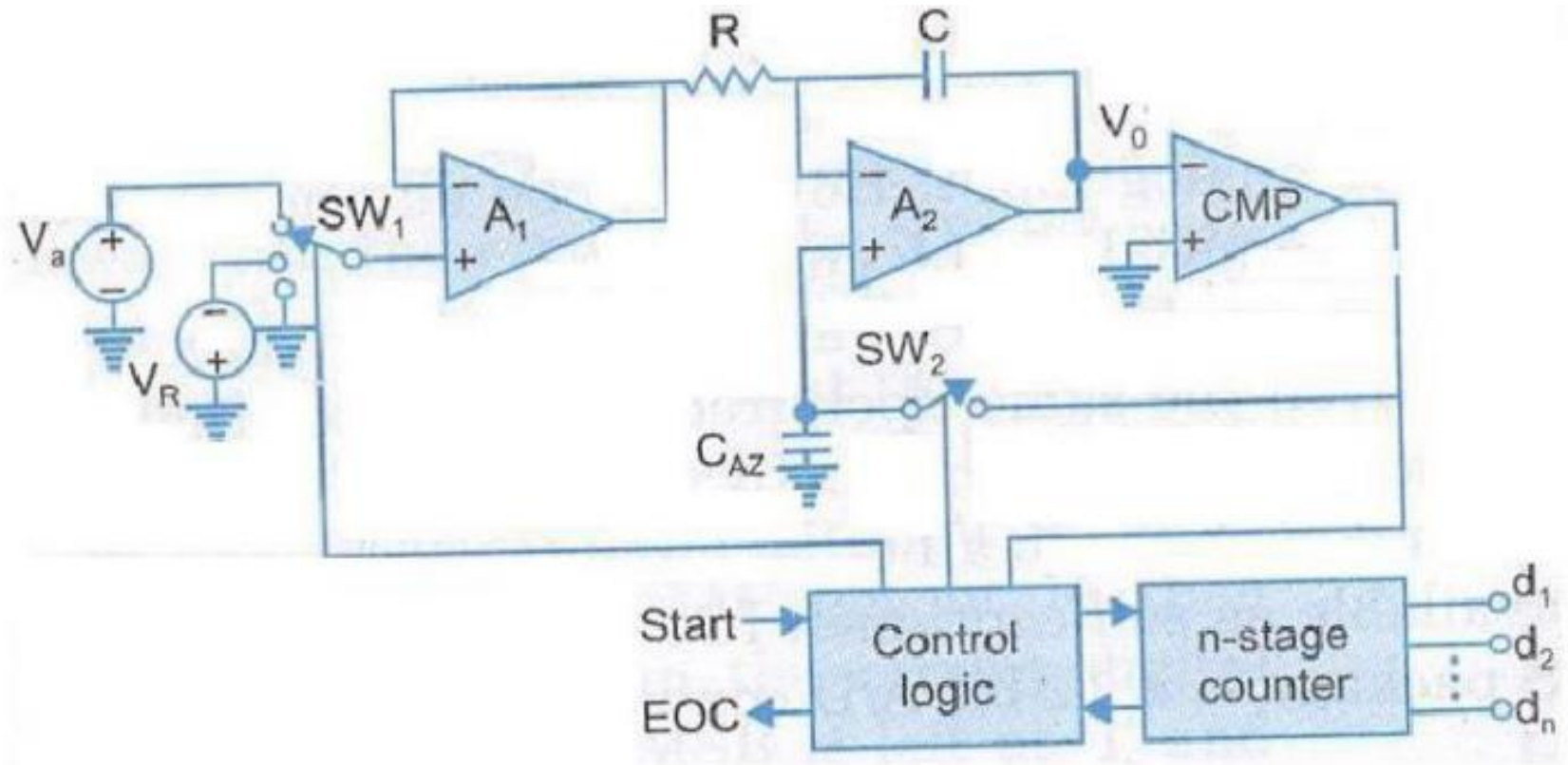
3.A DAC to convert the ith approximation xi to a voltage.

4.A Comparator to perform the function s(xi - x) by comparing the DAC's voltage with the input voltage.

5.A Register to store the output of the comparator and apply xi-1 - s(xi-1 - x)/2i.

- A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved.
- At each step in this process, a binary value of the approximation is stored in a successive approximation register (SAR). The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons.
- For example if the input voltage is 60 V and the reference voltage is 100 V, in the 1st clock cycle, 60 V is compared to 50 V (the reference, divided by two. This is the voltage at the output of the internal DAC when the input is a '1' followed by zeros), and the voltage from the comparator is positive (or '1') (because 60 V is greater than 50 V).
- At this point the first binary digit (MSB) is set to a '1'. In the 2nd clock cycle the input voltage is compared to 75 V (being halfway between 100 and 50 V: This is the output of the internal DAC when its input is '11' followed by zeros) because 60 V is less than 75 V, the comparator output is now negative (or '0'). The second binary digit is therefore set to a '0'. In the 3rd clock cycle, the input voltage is compared with 62.5 V (halfway between 50 V and 75 V: This is the output of the internal DAC when its input is '101' followed by zeros).
- The output of the comparator is negative or '0' (because 60 V is less than 62.5 V) so the third binary digit is set to a 0. The fourth clock cycle similarly results in the fourth digit being a '1' (60 V is greater than 56.25 V, the DAC output for '1001' followed by zeros). The result of this would be in the binary form 1001. This is also called *bit-weighting conversion*, and is similar to a binary search.

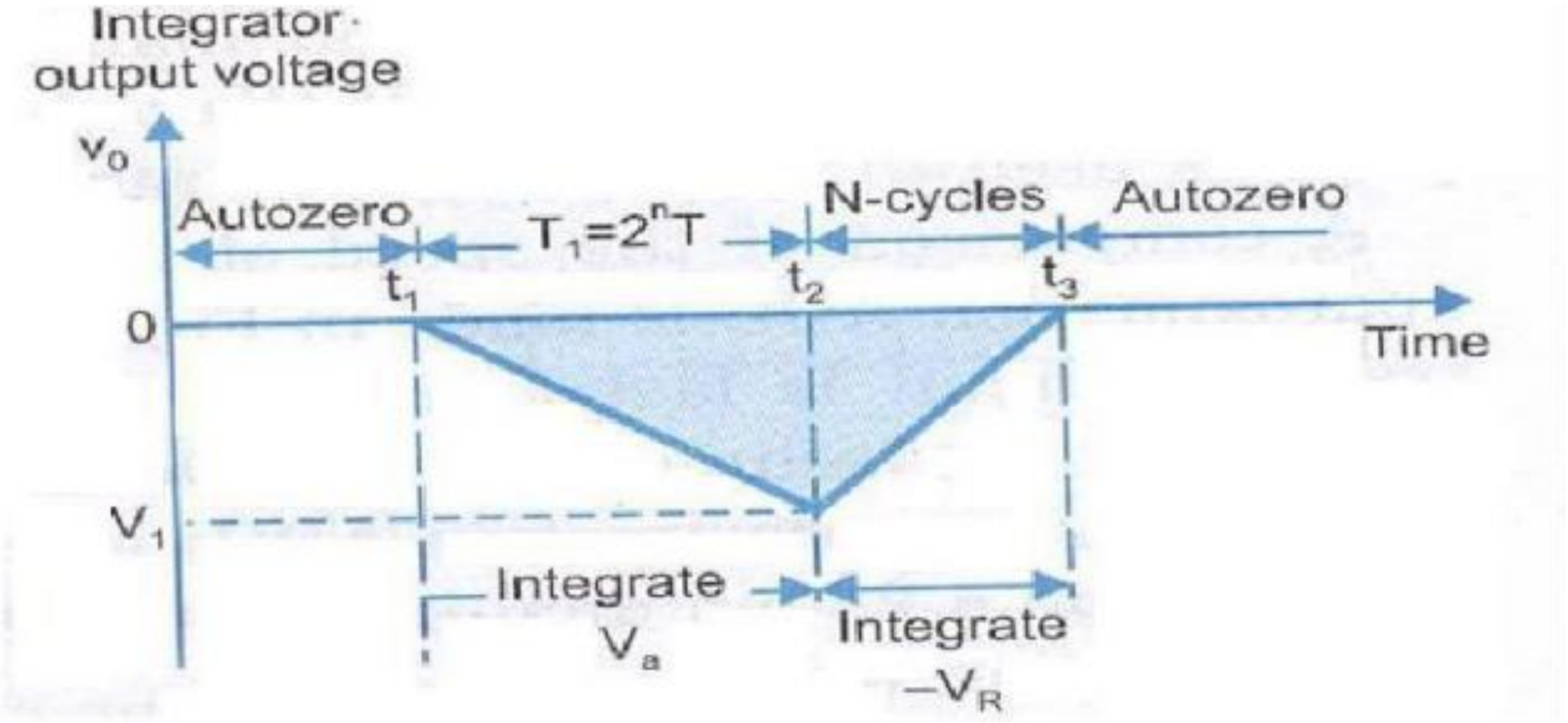
- The analogue value is rounded to the nearest binary value below, meaning this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired.
- The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz would be required. ADCs of this type have good resolutions and quite wide ranges. They are more complex than some other designs.



- An integrating ADC (also **dual-slope** ADC) shown in fig 2.25

(a.) applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period).

- Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period).
- The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period.
- The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution.
- Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.



- In operation the integrator is first zeroed (close SW2), then attached to the input (SW1 up) for a fixed time *M* counts of the clock (frequency 1/*t*). At the end of that time it is attached to the reference voltage (SW1 down) and the number of counts *N* which accumulate before the integrator reaches zero volts output and the comparator output changes are determined.

- In operation the integrator is first zeroed (close SW2), then attached to the input (SW1 up) for a fixed time *M* counts of the clock (frequency 1/*t*). At the end of that time it is attached to the reference voltage (SW1 down) and the number of counts *N* which accumulate before the integrator reaches zero volts output and the comparator output changes are determined.

$$T_1 = t_2 - t_1 = \frac{2^n\ counts}{clock\ rate}$$

And

$$t_3 - t_2 = \frac{digitalcountN}{clockrate}$$

For an integrator,

$$\Delta V_O = \frac{-1}{RC} V(\Delta t)$$

The voltage Vo will be equal to V1 at the instant t2 and can be written as

$$V_1 = \frac{-1}{RC} V_a(t_2 - t_1)$$

The voltage V1 is also given by

$$V_1 = \frac{-1}{RC}(-V_R)(t_2 - t_3)$$

So,

$$V_a(t_2 - t_1) = (V_R)(t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$ and, we get

$$V_a(2^n) = (V_R)N$$

Or,

$$V_a = (V_R)\left(\frac{N}{2^n}\right)$$

SPECIFICATIONS FOR DAC/ADC

- **1. RESOLUTION:** The Resolution of a converter is the smallest change in voltage which may be produced at the output of the converter.

Resolution (in volts)= (VFS) / (2^n-1)= 1 LSB increment

Ex: An 8-bit D/A converter have 28-1=255 equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range.

An 8-bit DAC is said to have: 8 bit resolution

:a resolution of 0.392 of full scale

:a resolution of 1 part in 255

Similarly the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output.

Ex: the input range of 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10V input range is 39.22 mV = (10V/255)

Ex: the input range of 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10V input range is 39.22 mV = (10V/255)

2. LINEARITY: The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal characteristics.

GLITCHES (PARTICULARLY DAC): In transition from one digital input to the next, like **0111 to 1000, it may effectively go through 1111 or 0000, which produces —unexpected‖** voltage briefly. If can cause problems elsewhere.

4. ACCURACY: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.

5. MONOTONIC: A monotonic DAC is the one whose analog output increases for an increase in digital input. It is essential in control applications. If a DAC has to be monotonic, the error should de lessthan ±(1/2) LSB at each output level.

6. SETTLING TIME: The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input. It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances.

Its ranges from 100ns to **10µs.**

7. STABILITY: The performance of converter changes with temperature, age and power supply variations. So the stability is required.

End